Butterfly Microcontroller Performance Supplement

(to the Butterfly Microcontroller Handbook publication no. HB4100)

INDUSTRIAL TEMPERATURE SPECIFICATION: -40º to 85º C

Supply ranges: 5.0 Volts +/-10%

3.3 Volts +/-0.3

Issue 1

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Table of Contents

Introduction

The following data supplied should be referenced in conjunction with the Butterfly Microcontroller Handbook publication no. HB4100.

This Timing Supplement gives performance figures over industrial (-40 to 85ºC) temperature ranges.

DC Parameters

Table 1: Absolute maximum ratings

Symbol	Parameter	min	max	Units
VDD	Supply Voltage	-0.5	7.0	V
Vip	Voltage applied to any pin	VSS-0.5	VDD+0.5	V
Osct	Output short circuit time		1	second
ESD	HBM model ESD		4	KV
Ts	Storage temperature	-40	125	deg C

Note: These are stress ratings only and exceeding the absolute maximum ratings may permanently damage the device. Operating the device at the absolute maximum ratings for extended periods may also affect the device reliability.

Table 2: DC operating conditions

Symbol	Parameter	3 Volt		5 Volt		Units
		min	max	min	max	
VDD	Supply Voltage	3.0	3.6	4.5	5.5	V
Ta	Ambient operating temperature	-40	85	-40	85	deg.C
I_{lu}	DC latch-up current	>500		>500		mA

Note: “3 Volt” denotes 3.3 Volt nominal operation.

Electrical Characteristics for Device Input/Output

All inputs, outputs and bidirectional signals are CMOS/TTL compatible, with the characteristics shown below.

Table 3: Device output pin characteristics

Parameter	Description	min	Typical	max	Condition
V_{OH}	Output High Voltage	$0.8V_{DD}$	$0.9V_{DD}$		3v: I_{OH}=2mA 5V I_{OH}=6mA
V_{OL}	Output Low Voltage		0.2V	0.4V	3v: I_{OL}=3mA 5V I_{OL}=6mA
O_{SC5}	Output short circuit current 5V supply	41	82	164mA	V_{DD}=5.5V
O_{SC3}	Output short circuit current 3V supply	16	32	64mA	V_{DD}=3.3V

Table 4: Device Input pin characteristics

Parameter	Description	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Units
V_{IH}	Input High Voltage	1.5		2.0		V
V_{IL}	Input Low Voltage		0.4		0.8	V
I_L	Input leakage current	-1	1	-1	1	µA
C_{IN}	Input (and I/O) Capacitance		6		6	pF

Note: All data and address inputs have on-chip circuitry to prevent oscillation if left unconnected. If it is intended to tie these inputs either high or low, a resistor value of less than 15k ohms should be used. The **Snreset** input pin has an internal pull-up resistor of typically 110k Ohms (minimum value of 50k Ohms) tied to it

AC Parameters

Loading Effects on Output Timing

Each timing parameter for external outputs within this document assume a 50pF load capacitance. This table can be used to calculate timings for alternative loads.

Table 5: Variances to output timing

Parameter	3 Volt value	5 Volt value	units	Description and notes
T_{RFF}	52	32	pS/pF	Maximum output timing adjustment for Variance from 50pF loads (falling edges)
T_{RFR}	130	80	pS/pF	Maximum output timing adjustment for variance from 50pF loads (rising edges)

Power Consumption

Typical active power is heavily dependent upon the application environment. Loads on output pins, system clock speed and activity, core activity and on-chip peripheral usage over time will all significantly impact this figure. The values given below assume constant operation of the ARM core plus typical activity expected using peripheral macro-functions, with Sclk @ 27MHz 5v nominal and @17MHz 3v nominal.

Table 6: Device Power consumption

Symbol	Condition	3 volt nominal	5 volt nominal	Units
PD	Typical active power consumption	100[1]	350[2]	mW
PD	Static power consumption	15[3]	15	µA

Note[1]. Sclk@17Mhz

Note[2]. Sclk@27Mhz

Note[3]. Sclk@0 Mhz and Pllpd=1 (High)

AC Performance:

The timing parameters on the following pages assume a logic switching point of 50% of VDD: Minimum (min) and maximum (max) figures are referenced at extremes of Voltage and Temperature.

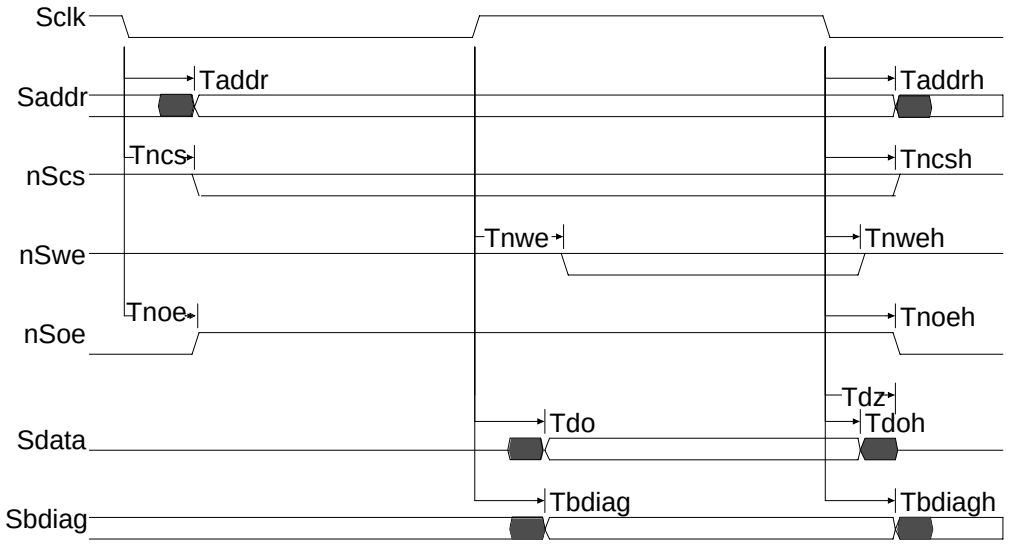
Important Notes:

All parameters will scale from their MIN to MAX value as temperature RISES or voltage FALLS. Their relationship, however, will always remain the same. Therefore if conditions give rise to a maximum propagation delay, such as **Taddr** (max), any corresponding hold times will also be maximum e.g. **Tnsweh** (max).

When using the PLL in Sync mode, the clock applied to the external **Sclk** pin on Butterfly (which will typically have an uneven mark-space ratio) will be re-shaped to produce an even mark-space ratio clock internally to the device. For simplicity however, throughout this document, all timing diagrams are shown with **Sclk** having an even mark-space ratio.

All timings for Butterfly in this document are final production figures.

MPC Timing Diagrams: On-Chip Wait-State Control



MPC External Memory Write Cycle

MPC External Memory Read Cycle

Note: For these transactions it is assumed that the ARM core is the current bus master. See DMA timings for any variance caused by other bus masters.

Table 7: MPC timing : PLL in SYNC mode

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Tspeed	62		38		ns	Sclk clock period
Taddr[2]	4	37	6	23	ns	Sclk to Address Valid 32 bit memory configurations
Taddr[3]	4	39	6	25	ns	Sclk to Address Valid all memory configurations
Taddrh[1]	1	25	2	18	ns	Address hold after Sclk
Tncs	6	37	6	23	ns	Sclk to chip select valid
Tncsh[1]	-1	25	1	18	ns	Chip select hold after Sclk
Tnoe	7	41	7	27	ns	Sclk to output enable active
Tnoeh	1	25	2	18	ns	Output enable hold after Sclk
Tnwe	-1	21	0	15	ns	Sclk to Write enable
Tnweh[1]	-2	19	0	14	ns	Write enable hold after Sclk
Tdisu	10	10	5	5	ns	Data setup before Sclk
Tdih	0	10	0	7	ns	Data input hold time
Tdo	5	41	6	25	ns	Data valid time after Sclk
Tdz	16	37	8	22	ns	Data disable time after Sclk
Tdoh	-1	21	0	14	ns	Data out hold time after Sclk
Tbdiag	0	27	2	16	ns	Bdiag data valid after Sclk
Tbdiagh	-2	18	0	13	ns	Bdiag output data hold time after Sclk

Note[1]. Tnweh (nSwe rising) will ALWAYS precede Taddrh and Tncsh.

Note[2]. This value is correct for 32 bit memory configurations ONLY. i.e. it does NOT include Half-word and Byte Selects (i.e: Sadd1 & Sadd0).

Note[3]. This value is correct for ALL memory configurations. i.e. it does include Half-word and Byte Selects (i.e: Sadd1 & Sadd0).

Table 8: MPC timing : PLL in MULTIPLY mode.

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Tspeed	60	110	38	100	ns	Sclk clock period
Taddr[2]	-6	27	-2	15	ns	Sclk to Address Valid 32 bit memory configurations
Taddr[3]	-6	29	-2	17	ns	Sclk to Address Valid all memory configurations
Taddrh[1]	-19	1	-12	2	ns	Address hold after Sclk
Tncs	-4	27	-2	15	ns	Sclk to chip select valid
Tncsh[1]	-21	1	-13	2	ns	Chip select hold after Sclk
Tnoe	-3	27	-1	17	ns	Sclk to output enable active
Tnoeh	-19	1	-12	2	ns	Output enable hold after Sclk
Tnwe	-11	7	-8	5	ns	Sclk to Write enable
Tnweh[1]	-22	-5	-14	-2	ns	Write enable hold after Sclk
Tdisu	30	30	19	19	ns	Data setup before Sclk
Tdih	-16	-4	-11	-3	ns	Data input hold time
Tdo	-5	47	-2	15	ns	Data valid time after Sclk
Tdz	26	23	0	12	ns	Data disable time after Sclk
Tdoh	-21	-3	-14	-2	ns	Data out hold time after Sclk
Tbdiag	-10	13	-6	6	ns	Bdiag data valid after Sclk
Tbdiagh	-22	-6	-14	-3	ns	Bdiag output data hold time after Sclk

Note[1]. Tnsweh (nSwe rising) will ALWAYS precede Taddrh and Tncsh.

Note[2]. This value is correct for 32 bit memory configurations ONLY. i.e. it does NOT include Half-word and Byte Selects (i.e: Sadd1 & Sadd0).

Note[3]. This value is correct for ALL memory configurations. i.e. it does include Half-word and Byte Selects (i.e: Sadd1 & Sadd0).

Table 9: MPC timing : PLL in BYPASS model

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Tsclkl[4]	31		19		ns	Sclk low period
Tsclkh[4]	18		13		ns	Sclk high period
Tspeed[4]	62		38		ns	Sclk clock period
Taddr[2]	15	48	13	30	ns	Sclk to Address Valid (32 bit memory configurations)
Taddr[3]	15	50	13	32	ns	Sclk to Address Valid (all memory configurations)
Taddrh,[1]	12	32	9	23	ns	Address hold after Sclk
Tncs	17	48	13	30	ns	Sclk to chip select valid
Tncsh[1]	10	32	8	23	ns	Chip select hold after Sclk
Tnoe	18	48	14	32	ns	Sclk to output enable active
Tnoeh	12	32	9	23	ns	Output enable hold after Sclk
Tnwe	10	28	7	20	ns	Sclk to Write enable
Tnweh[1]	9	26	7	19	ns	Write enable hold after Sclk
Tdisu	-1	-1	-2	-2	ns	Data setup before Sclk
Tdih	5	17	4	12	ns	Data input hold time
Tdo	16	48	13	30	ns	Data valid time after Sclk
Tdz	27	44	15	27	ns	Data disable time after Sclk
Tdoh	10	28	7	19	ns	Data out hold time after Sclk
Tbdiag	11	34	9	21	ns	Bdiag data valid after Sclk
Tbdiagh	9	25	7	18	ns	Bdiag output data hold time after Sclk

Note[1]. Tnsweh (nSwe rising) will ALWAYS precede Taddrh and Tncsh.

Note[2]. This value is correct for 32 bit memory configurations ONLY. i.e. it does NOT include Half-word and Byte Selects (i.e: Sadd1 & Sadd0).

Note[3]. This value is correct for ALL memory configurations. i.e. it does include Half-word and Byte Selects (i.e: Sadd1 & Sadd0).

Note[4]. Tspeed (min) assumes an even MARK:SPACE ratio clock. If an uneven ratio is used then Tspeed (min) can be determined by Tsclkl (min) and Tsclkh (min).

Example SRAM Access Time Requirements.

The following table shows some example SRAM access timing requirements (**Taa**) to allow single cycle read/write operations at different operating frequencies. These examples are designed to indicate the memory requirements in order to gain maximum performance. They are true for Bypass and Sync PLL operating modes. (If the Microcontroller is to be used with slower memory then access wait states should be added as required. It should be remembered that 32 bit memory configurations do not preclude sub memory-width reads and writes.

Details of how to arrange and calculate System memory requirements are given in the MPC Chapter of the Butterfly Microcontroller Handbook publication no. HB4100.

Table 10: Typical SRAM speed vs operating frequency.

Typical supply voltage	Typical operating frequency (Sclk)	Typical SRAM (Taa) requirement (32 bit memory configurations)	Typical SRAM (Taa) requirement (all memory configurations)
5.0 v	26 MHz	10 ns	8ns
5.0 v	25 MHz	12 ns	10 ns
5.0 v	23 MHz	15 ns	13 ns
5.0 v	22 MHz	17 ns	15 ns
5.0 v	18 MHz	25 ns	23 ns
3.3 v	16 MHz	15 ns	13 ns
3.3 v	14 MHz	23 ns	20 ns

MPC Timing Diagram Showing Off-chip Wait-state Control

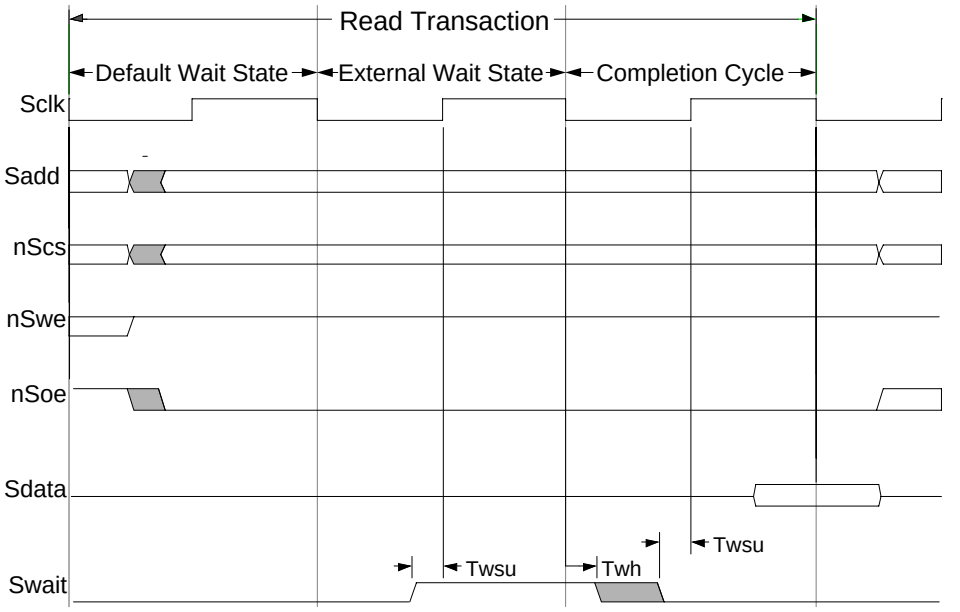


Table 11: MPC Timing: Swait with the PLL in SYNC modell

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	units	Description and notes
Twsu	9		5		ns	Swait setup time before Sclk
Twh	8		6		ns	Swait hold time after Sclk

Table 12: MPC Timing: Swait with the PLL in MULTIPLY mode

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	units	Description and notes
Twsu	29		19		ns	Swait setup time before Sclk
Twh	-6		-4		ns	Swait hold time after Sclk

Table 13: MPC Timing: Swait with the PLL in BYPASS mode

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	units	Description and notes
Twsu	-2		-2		ns	Swait setup time before Sclk
Twh	15		11		ns	Swait hold time after Sclk

Watchdog Timer Timing Diagram

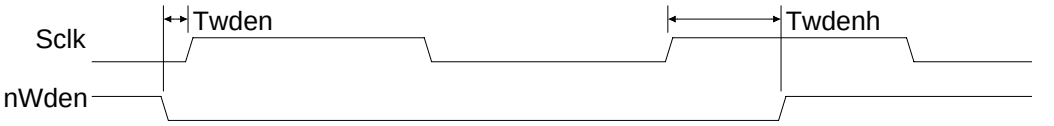


Table 14: Watchdog Timer: nWden timing, PLL in SYNC mode

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Twden	7		4		ns	Watchdog enable setup time before Sclk
Twdenh	8		6		ns	Watchdog enable hold time after Sclk

Table 15: Watchdog Timer: nWden timing, PLL in MULTIPLY mode

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Twden	27		18		ns	Watchdog enable setup time before Sclk
Twdenh	-6		-4		ns	Watchdog enable hold time after Sclk

Table 16: Watchdog Timer: nWden timing, PLL in BYPASS mode

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Twden	-4		-3		ns	Watchdog enable setup time before Sclk
Twdenh	15		11		ns	Watchdog enable hold time after Sclk

Timer Counter Timing Diagrams:

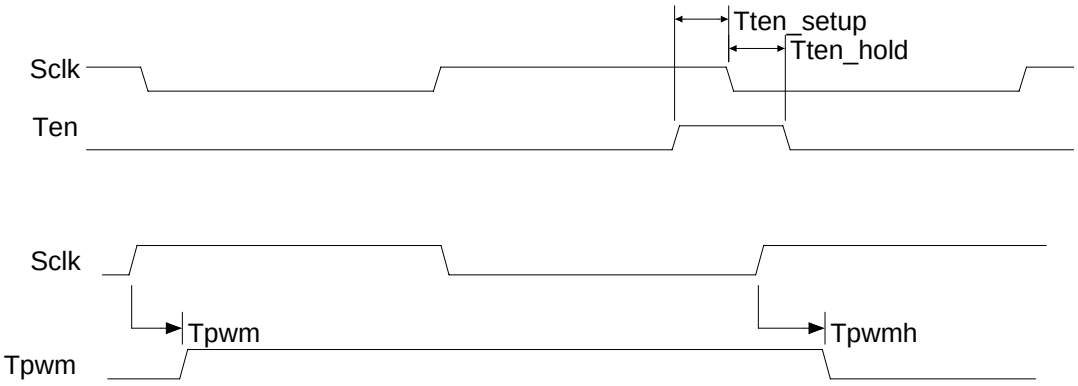


Table 17: Timer Counter with the PLL in SYNC mode

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Tten_setup	7		3		ns	Timer enable setup time before Sclk
Tten_hold	8		6		ns	Timer enable hold time after Sclk
Tpwm		40		28	ns	PWM output delay after Sclk
Tpwmh	8		7		ns	PWM hold time after Sclk

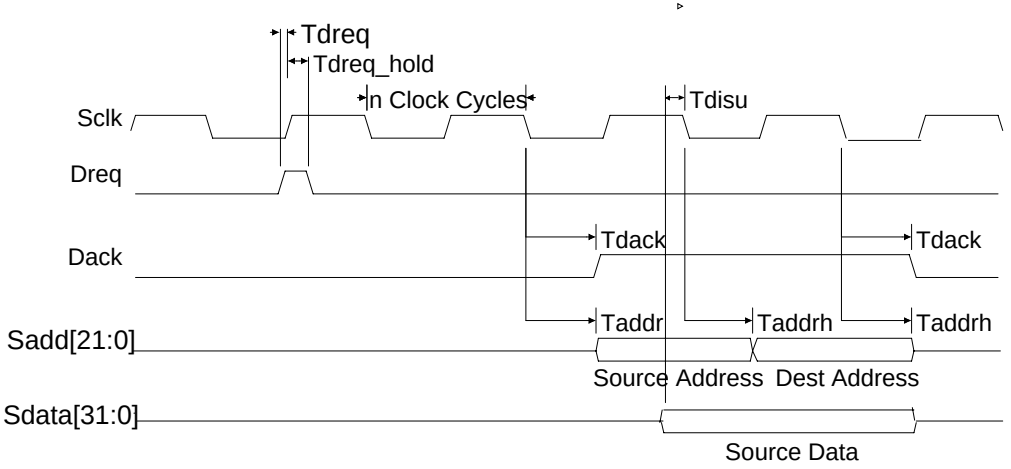
Table 18: Timer Counter with the PLL in MULTIPLY mode

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Tten_setup	27		17		ns	Timer enable setup time before Sclk
Tten_hold	-6		-4		ns	Timer enable hold time after Sclk
Tpwm		26		18	ns	PWM output delay after Sclk
Tpwmh	-12		-7		ns	PWM hold time after Sclk

Table 19: Timer Counter with the PLL in BYPASS mode

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Tten_setup	-4		-4		ns	Timer enable setup time before Sclk
Tten_hold	15		11		ns	Timer enable hold time after Sclk
Tpwm		47		33	ns	PWM output delay after Sclk
Tpwmh	19		14		ns	PWM hold time after Sclk

DMA timing: Dual Address Transfer.



NOTE: When performing a DMA transfer, memory signals are as per the MPC timing information.

Table 20: DMA through MPC: PLL in SYNC mode

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Tdreq	7		4		ns	Dreq setup before Sclk
Tdreq_hold	4		3		ns	Dreq hold time after Sclk
Tdack		29		20	ns	Sclk to Dack active

Table 21: DMA through MPC: PLL in MULTIPLY mode

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Tdreq	27		18		ns	Dreq setup before Sclk
Tdreq_hold	-10		-7		ns	Dreq hold time after Sclk
Tdack		15		4	ns	Sclk to Dack active

Table 22: DMA through MPC:PLL in BYPASS mode

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Tdreq	-4		-3		ns	Dreq setup before Sclk
Tdreq_hold	11		8		ns	Dreq hold time after Sclk
Tdack		36		25	ns	Sclk to Dack active

Programmable Peripheral Interface Timing Diagram

Note: Parallel port timings are the same for all PLL modes.

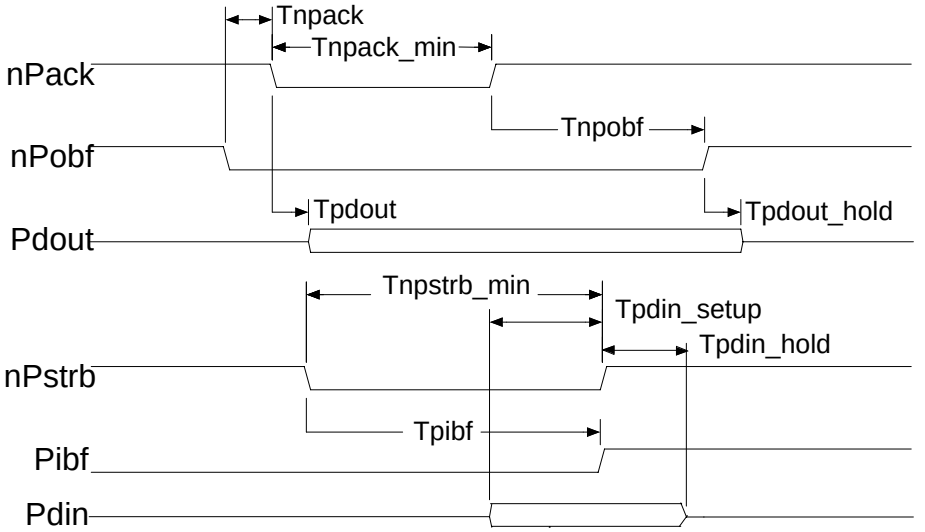


Table 23: Programmable Peripheral Interface: ALL modes

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Tnpack	0		0		ns	nPack setup time after nPobf.
Tnpack_min	Tspeed*/2		Tspeed*/2		ns	nPack pulse width.
Tpdout		24		16	ns	Pdata valid after nPack.
Tnpobf	0	Tspeed*	0	Tspeed*	ns	nPobf reset after nPack.
Tpdout_hold	0		0		ns	Pdata hold after nPobf
Tpdin_setup	5		5		ns	Data-in setup time before nPstrb
Tpdin_hold	5		5		ns	Data-in hold time after nPstrb.
Tnpstrb_min		Tspeed*		Tspeed*	ns	nPstrb pulse width.
Tpibf		Tspeed* +28		Tspeed* +20	ns	Pibf valid after nPstrb.

Note[8]. Tspeed equals the period of Sclk.

External Interrupt Inputs: Timing for Edge Sensitivity Mode

Notes:

Interrupts are asynchronous and therefore unaffected by the PLL modes.
Interrupts are programmable and timings are apply for both rising and falling edges.

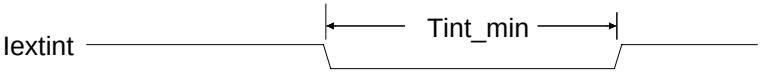


Table 24: Edge triggered interrupts: Extint (1 or 2), PLL (All modes)

Parameter	3 Volt min	3 Volt max	5 Volt min	5 Volt max	Unit	Description and notes
Tint_min	33		22		ns	Minimum external interrupt width

External interrupt inputs: Timing for Level sensitivity mode

When Level-sensitive interrupts are programmed, they must remain active until a suitable response is generated. i.e. until they have been serviced. Therefore please refer to Butterfly Handbook for timing relationship diagrams.

UART External clock input: Ueclk

The Maximum recommended frequency of the external UART clock is the same value of Sclk.

Device I/O Summary

The following table gives a summary of all the pins on Butterfly together with a reference to the relevant Butterfly Microcontroller Handbook Chapter and the appropriate section (if applicable) within this Performance Supplement.

Mnemonic	Type	Function	Notes/Data Supplement reference	Handbook Chapter(s)
Dreq1,2	I	DMA Request	See DMA Timing & System Configuration register	Introduction, DMA
Dack1,2	O	DMA Acknowledge	See DMA Timing	DMA
Sclk	I/O	System clock I/O	IN = PLL in Bypass OR Sync OUT = Crystal Oscillator used	PLL
nSreset	I	0 = System Reset	Includes 100k pullup	POCO
Sdata31:0	I/O	Data I/O	See MPC Timing	MPC
Sadd21:0	I/O	Address Outputs for external memory	Always active Outputs unless Test pin is high.	MPC
nScs3:0	O	0 = Chip select for external memory	See MPC Timing	MPC
nSwe3:0	O	0 = Write enable for external memory	See MPC Timing	MPC
nSoe	O	0 = Output enable for external memory	See MPC Timing	MPC
Swait	I	1 = Wait state requested	See Swait Timing	MPC
Srsize1:0	I	Reset Bus Size	00 = 8 bit Bus Size 01 = 16 bit Bus Size 1X = 32 bit Bus Size	MPC
Sbigendian	I	Endian select for external memory	0 = little Endian 1 = Big Endian	MPC
Ten1,2	I	1 = Timer Enabled	See Timer Counter Timing	Timer/Counter
Tpwm	O	Timer PWM output	See Timer Counter Timing	Timer/Counter
nWden	I	0 = Watchdog enabled	See Watchdog Timing	Watchdog
Utxd1,2	O	UART Transmit Data		UART

Mnemonic	Type	Function	Notes/Data Supplement reference	Handbook Chapter(s)
Urxd1,2	I	UART Receive Data		UART
Ueclk/ Udcd1,2	I	UART external Clock OR Data Carrier Detect	Functionality set using System Configuration Register.	Introduction, UART
nUrts1,2	O	0 = UART ready to send.		UART
nUcts1,2	I	0 = UART is clear to send		UART
Pdat7:0	I/O	Parallel Port (PPI) Data.	See PPI Timing	PPI
nPstrb	I	0 = indicates data available. Rising edge latches data.	See PPI Timing	PPI
nPack	I	0 = Enable PPI Data output. 1 = Tristate PPI Data output.	See PPI Timing	PPI
nPobf	O	0 = PPI Data output buffer full	See PPI Timing	PPI
Pibf	O	1 = PPI Data input buffer full.	See PPI Timing	PPI
Iextint1,2	I	External interrupts - Fully programmable.	See Ext. Interrupt Timing & Interrupt Source Channels	Introduction, INTC
Bdiag3:0	O	Encoded Bus States.	See MPC Timing	BBM,MPC
Oscin/ Bypass	I	Crystal connection 1 OR PLL mode selection.	Crystal connection OR 0 = PLL Sync mode 1 = PLL Bypass mode	PLL
Oscout	O	Crystal connection 2.		PLL
Set_3V	I	VDD selection.	0 = For 5V Operation 1 = For 3V Operation	PLL
Oscen	I	Crystal Oscillator Control.	0 = Oscillator Disabled 1 = Oscillator Enabled	PLL
Pllpd	I	PLL power down.	0 = PLL operational 1 = PLL powered down	PLL, POCO